ABSTRACT

In addition to a first transmitter circuit 200, a plurality of transmission lines 800 and a first data processing circuit 600 in the receive side, so as to cause a DLL circuit 620 to be regulated that regulates timing of a sampling clock of the data signal, a second first transmitter circuit 300, a transmission line 900 and a second data processing circuit 700 are provided, when a second specific signal string is sent, a regulation start signal string is caused to be distributed by the second data processing circuit 700, regulation is caused to be made for a DLL circuit 620 of the first data processing circuit 600 by a regulation signal string, the data starting with the bit next to a first specific signal string detected in the data signal is written into a m-address n-bit FIFO circuit 660, simultaneously a read address synchronized with a system clock is generated from a third specific signal string that came to the second data processing circuit 700, whereby the data is recovered.